C128 DIAGNOSTIC INSTRUCTION AND TROUBLESHOOTING MANUAL ASSEMBLY #314060-01/02

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C128 DIAGNOSTIC OPERATION AND TEST INSTRUCTIONS

1.1 UNPACKING

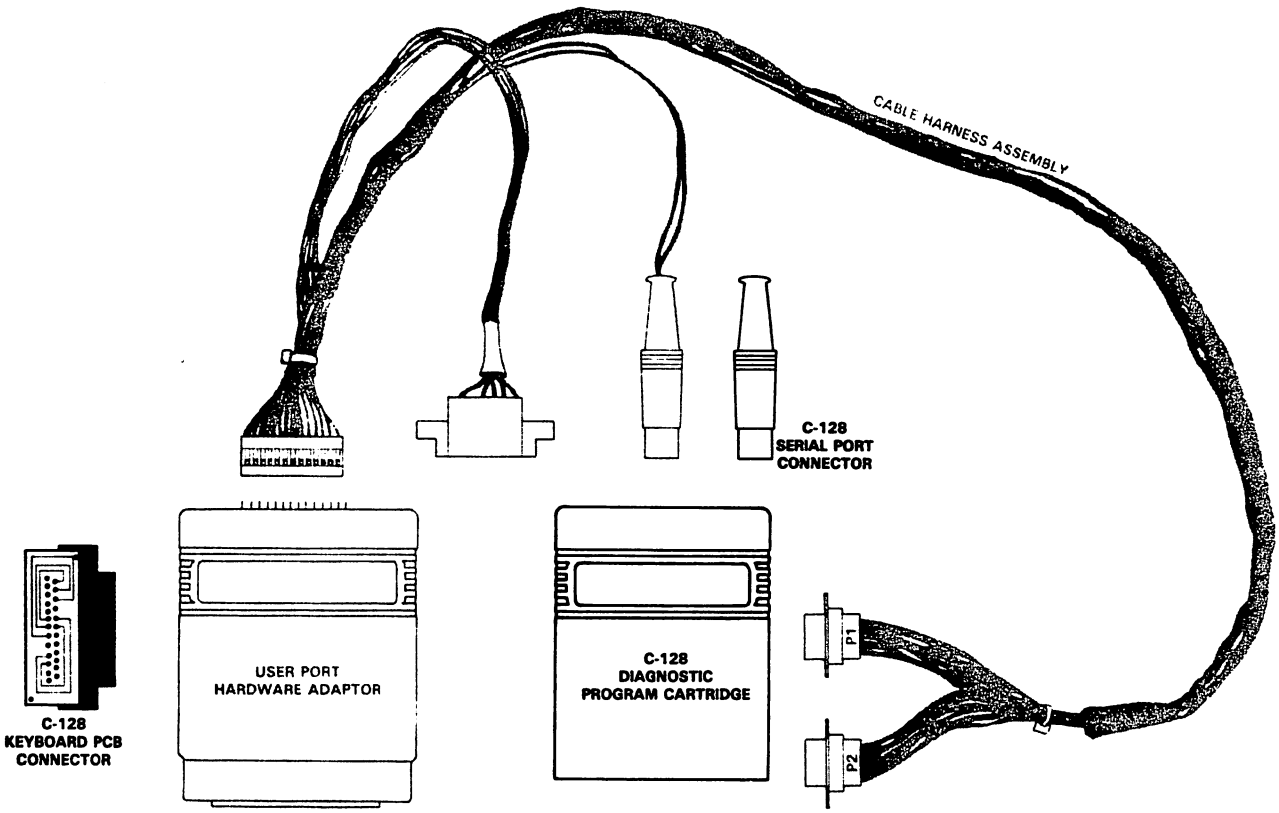
Depending on which of the C128 Diagnostic Assemblies received, it should include 1 each of the following:

C128 DIAGNOSTIC ASSEMBLY (ADD-ON) P/N 314060-02

- Diagnostic Program Cartridge
- Keyboard Connector PCB
- Serial Port Connector

C128 DIAGNOSTIC ASSEMBLY (COMPLETE) P/N 314060-01

- Diagnostic Program Cartridge
- User Port Hardware Adapter
- Keyboard Connector PCB
- Cable Harness Assembly
- Serial Port Connector



The User Port Hardware Adapter and Cable Harness Assembly (gray shaded assemblies) used with the C128 Diagnostic are the same as used with the C64 Diagnostic with the exception of the Keyboard Connector PCB and the Serial Port Connector (black outlined assemblies).

1.2 BASIC DIAGNOSTIC THEORY

The Diagnostic Program Cartridge resides at memory location $8000-$9D5F. When the C128 is turned on, memory locations $8006-$8009 are read. If these locations contain the characters '2CBM', the program contained in the Diagnostic Cartridge is executed. The Diagnostic exercises the 8502 MPU, System RAM, ROM and Internal I/O Circuits of the C128. The test being executed, status (OK or BAD), and possible IC failure will be displayed.

1.3 AUTOMATIC DIAGNOSTIC UPDATES

From time to time Commodore may find it necessary to change the Hardware and/or Software of the C128 System. If these changes effect the operation of the Diagnostic it will be necessary to send updates to all Authorized Service Locations. These updates may be in the form of a diskette or possibly a Diagnostic EPROM. These updates will be shipped automatically and the Servicing Facility will be billed a nominal fee to cover the cost of material and handling.

1.4 INSTALLATION

1.4.1 Make sure the POWER is OFF on the C128.

1.4.2 Plug the DIAGNOSTIC PROGRAM CARTRIDGE into the EXPANSION PORT. (CN1)

- Make sure the label, C128 Diagnostic, is facing up.

1.4.3 Plug the CABLE HARNESS ASSEMBLY into the connector located on the back of the USER PORT HARDWARE ADAPTER.

- If using the C128 DIAGNOSTIC ASSEMBLY (ADD-ON) — the CABLE HARNESS ASSEMBLY and the USER PORT HARDWARE ADAPTER used must be taken from the C64 Diagnostic Kit.
- If using the C128 DIAGNOSTIC ASSEMBLY (COMPLETE) — the CABLE HARNESS ASSEMBLY and the USER PORT HARDWARE ADAPTER used are included. The connector is KEYED to allow it to be connected only one way. However, it is very easy to miss a row of pins, so care should be taken when connecting the harness.

1.4.4 Plug the USER PORT HARDWARE ADAPTER into the USER PORT (CN9).

- Make sure the LABEL AREA is facing up. (Cartridge screw down.)

1.4.5 Plug the 6-PIN EDGE CONNECTOR into the CASSETTE PORT (CN2).

- The Connector is keyed to allow it to be plugged in only one way.

1.4.6 Plug the 6-PIN DIN CONNECTOR into the SERIAL PORT (CN6).

- Use the detached 6-PIN DIN CONNECTOR. (Labeled C128)

1.4.7 Plug the two 9-PIN MINI DIN CONNECTORS into the CONTROL PORTS (CN3, CN4).

- It makes no difference which connector goes to which port.

1.4.8 Check to make sure all the connectors are installed correctly.

- DO NOT INSTALL THE KEYBOARD CONNECTOR PCB until the Diagnostic Tests are running.
- The KEYBOARD CONNECTOR PCB NEED NOT be installed to run the Diagnostic.

1.4.9 Make sure the 40/80 key is in the proper position for the tests you wish to execute.

- 40/80 key in the up position — All Diagnostic Tests are executed.
- 40/80 key in the down position — All RAM Testing is Bypassed System ROM and I/O Testing Only.

1.4.10 Turn the POWER ON to the C128.

1.5 DIAGNOSTIC STARTUP

The Diagnostic Test should 'Auto-Boot' on System Power Up and begin executing the Diagnostic Tests. If no screen is displayed, it is an indication that the System has an Initial Start-up Problem. If this is the case, refer to C128 System Troubleshooting — Section 2 of this manual.

If the C128 executes the Initial Startup Sequence correctly, the current test being executed will be displayed. If an internal circuit fails the test, a 'BAD' message will be displayed next to the failed test and a probable IC failure indicated inside the 'Red' rectangular box. If the internal circuit being tested passes the test, an 'OK' message is displayed next to the test.

It is possible to have a problem with the C128 that is not a constant or hard failure. It may pass a test one time and fail the next. If a failure is detected, a 'BAD' message will be displayed in 'Red' next to the failed test and a probable IC failure indicated inside the 'Red' rectangular box. If the test passes on the next diagnostic cycle, the 'OK' message is displayed in 'Red' next to the test and the probable IC failure indication will not be cleared from the box. This is an indication that a failure occurred at least once during diagnostic run time.

Once the Diagnostic is running it will continue to execute, displaying the results of the tests, count (number of cycles run), and 2 Time of Day clocks. A detailed description of these clocks is contained in section 1.7.17 Lower Screen Display of this manual.

1.6 DIAGNOSTIC TEST DESCRIPTION

1.6.1 ZERO PAGE TEST

Zero Page Memory resides at locations $0000-$00FF. Two of the locations are reserved for the 8502 MPU I/O Port (used primarily for C64 mode). Location $0000 is the 8502 Data Direction Register and location $0001 is the Data Register. Memory locations $0002-$000C are reserved by the diagnostic for such things as storing the number of cycles, diagnostic mode, etc. The Zero Page Test writes HEX 00, 55, AA and FF into locations $000D-$00FF. A test byte is set and walked through zero page memory to check for stuck bytes. The data is read and compared to stored data. If DATA READ = DATA STORED, zero page RAM is 'OK'. If DATA READ ≠ DATA STORED, zero page RAM is 'BAD'.

If a RAM failure occurs during the Zero Page Test, any indicated RAM IC must be replaced before the diagnostic test is allowed to proceed. RAM failures in this area will normally display erroneous results in the remaining tests.

If this does not correct the problem, or if more than two RAM ICs are displayed defective, refer to C128 System Troubleshooting — Sections 2.6 thru 2.7 — Troubleshooting the 4116 System RAM.

1.6.2 STACK PAGE TEST

Stack Page Memory resides at locations $0100-$01FF. The Stack Page Test writes HEX 00, 55, AA and FF into locations $0100-$01FF. A test byte is set and walked through stack page memory to check for stuck bytes. The data is read and compared to stored data. If DATA READ = DATA WRITTEN, stack page RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, stack page RAM is 'BAD'.

If a RAM failure occurs during the Stack Page Test, any indicated RAM IC must be replaced before the diagnostic test is allowed to proceed. RAM failures in this area will normally display erroneous results in the remaining tests.

If this does not correct the problem, or if more than two RAM ICs are displayed defective, refer to C128 System Troubleshooting — Sections 2.6 thru 2.7 — Troubleshooting the 4116 System RAM.

1.6.3 SCREEN RAM TEST

The Screen RAM resides at locations $0400-$07FF. The Screen RAM Test writes HEX 00, 55, AA and FF in locations $0400-$07FF one character position at a time. After a short delay, the data is read and compared to the written data. If DATA READ = DATA WRITTEN, screen RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, screen RAM is 'BAD'.

After the Screen RAM Test has completed a pass of one character, it replaces the character that was there previous to the test, if this character is distorted, it may be an indication of a Zero Page RAM problem, which should be displayed during the Zero Page Test of the next diagnostic cycle.

If an error occurs during the Screen Ram Test, any indicated RAM IC Failure should be replaced. If this does not correct the problem, or if more than two RAM ICs are displayed defective, refer to C128 System Troubleshooting — Sections 2.6 thru 2.7 — Troubleshooting the 4116 System RAM.

1.6.4 COLOR RAM TEST

The Color RAM resides at locations $D800-DC00. The Color RAM Test writes HEX 00, 55, AA, FF in these locations once color position at a time. After a short delay, the data is read and compared to the written data. If DATA READ = DATA WRITTEN, screen RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, screen RAM is 'BAD'.

After the Color RAM Test has completed a pass of one color, it will replace the color that was there previous to the test, if this color is distorted it may be an indication of a Zero Page RAM problem, which should be displayed during the Zero Page Test of the next diagnostic cycle.

If an error occurs during the Color RAM Test, any indicated RAM IC Failure should be replaced. If replacement of the indicated RAM IC does not correct the problem, or if more than two RAM ICs are displayed defective, refer to C128 System Troubleshooting — Sections 2.6 thru 2.7 — Troubleshooting the 4116 System RAM and C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

1.6.5 HI RAM BANK 0/HI RAM BANK 1 TESTS

Before the HI RAM BANK is tested, the diagnostic program is moved from ROM into the LO RAM BANK 0 area. The diagnostic writes HEX 00, 55, AA, FF in locations $4000-$FE00. A byte is set to walk a '1' bit through each of these locations. After this test is complete, the bit pattern is reversed so that a '0' bit is walked through each location. This is referred to as a 'Walking 1's and 0's Test'. In both tests the data is first written to all locations, and after a short delay to insure a refresh cycle, the data is then read back and compared to the test byte. If DATA READ = DATA WRITTEN, RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, RAM is 'BAD'.

If an error occurs during the HI RAM tests, any indicated RAM IC failure should be replaced. If replacement of the indicated RAM IC does not correct the problem, or if more than two RAM ICs are displayed defective, refer to C128 System Troubleshooting — Sections 2.6 thru 2.7 — Troubleshooting the 4116 System Ram.

1.6.6 LO RAM BANK 0/LO RAM BANK 1 TESTS

Before the LO RAM BANK is tested, the diagnostic program is moved from ROM into the HI RAM BANK 0 area. The diagnostic writes HEX 00, 55, AA, FF in locations $0800-$F000. A byte is set to walk a '1' bit through each of these locations. After this test is complete, the bit pattern is reserved so that a '0' bit is walked through each location. This is referred to as a 'Walking 1's and 0's Test'. In both tests the data is first written to all locations, and after a short delay to insure a refresh cycle, the data is then read back and compared to the test byte. If DATA READ = DATA WRITTEN, RAM is 'OK'. If DATA READ ≠ DATA WRITTEN, RAM is 'BAD'.

If an error occurs during the LO RAM tests, any indicated RAM IC failure should be replaced. If replacement of the indicated RAM IC does not correct the problem, or if more than two RAM ICs are displayed defective, refer to C128 System Troubleshooting — Sections 2.6 thru 2.7 — Troubleshooting the 4116 System RAM.

1.6.7 KERNAL/BASIC LO/BASIC HI/CHARACTER ROM TEST

All operating system ROMs are checked by adding the contents of each address to a value equal to the sum of the data in all the preceding addresses. This is referred to as a 'Checksum'. The checksum is displayed in HEX next to the ROM being tested. Any changes to the C128 operating system ROMs will be reflected by different checksums. The current ROM set checksums are:

LOCATION	DESCRIPTION	PART NUMBER	CHECKSUM
U18	Character	390059-01	FB
U33	Basic Lo	318018-02	91
U34	Basic Hi	318019-02	81
U35	Kernal	318020-03	81

If any ROM checksum result does not match the value in the table, the indicated ROM failure should be replaced. If replacement of the indicated ROM does not correct the problem, refer to C128 System Troubleshooting — Section 2.13 — Troubleshooting the 8721 PLA.

If updates are implemented to the current operating system ROM, the new checksum values will be distributed as Tech Topics.

1.6.8 PLA TEST

The PLA, Programmable Logic Array, contains all the address decoding logic for system RAM, ROM and I/O. The PLA test reads the first 4 bytes of data from the Character, Basic Lo, Basic Hi and Kernal ROMS. The data is compared to stored values in the diagnostic cartridge. If DATA READ = DATA STORED, the PLA is able to select all ROMS. The PLA test then tests the I/O select output by reading one location of color RAM comparing the data to a stored value in the diagnostic cartridge. If the Character ROM, Basic Lo ROM, Basic Hi ROM, Kernal ROM and Color RAM can all be selected, the PLA is 'OK'.

If the PLA is displayed 'BAD' it should be replaced. If this does not correct the problem, refer to C128 System Troubleshooting — Section 2.13 — Troubleshooting the 8721 PLA.

1.6.9 CASSETTE PORT TEST

The Cassette Port Test checks the cassette read and cassette sense inputs by outputting low pulses on the cassette sense line, which are read on the cassette read input. Cassette write and cassette motor outputs are checked by outputting low pulses on the cassette motor line, which are read on the cassette write line. If RECEIVED DATA = TRANSMITTED DATA, the cassette port is 'OK'. If TRANSMITTED DATA $\neq$ RECEIVED DATA, the cassette port is 'BAD'.

If a failure occurs during the Cassette Port Test, any indicated IC should be replaced. If this does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

ON THE ORIGINAL C128 PCB (REV. 6) THE CASSETTE PORT, SERIAL PORT AND IC U1 WILL ALWAYS DISPLAY 'BAD'. THIS IS DUE TO A 7407 TTL BUFFER, PCB LOCATION U60, WHICH WAS ADDED TO ALL PCB'S REV. 7 AND ABOVE.

1.6.10 KEYBOARD TEST

The Keyboard Matrix is scanned by a 6526 CIA, U1. During normal operation, 0 bits are output on Port A, PA0-PA7. If a key is depressed, a 0 bit is returned on Port B, PB0-PB7.

The Keyboard Test checks to see if the keyboard connector PCB is in place. If the connector is present, a binary count is output on Port A, PA0-PA7. This binary count is looped through the connector and input on Port B, PB0-PB7. The input count is read on Port B, and compared to the output count on Port A. If INPUT COUNT = OUTPUT COUNT, a binary count is ouput on Port B, PB0-PB7. This binary count is looped through the connector and input on Port A, PA0-PA7. The input count is read on Port A, and compared to the output count on Port B. If INPUT COUNT = OUTPUT COUNT, the keyboard is 'OK'. If INPUT COUNT ≠ OUTPUT COUNT, the keyboard is 'BAD'.

If the keyboard connector PCB is not in place, the Keyboard Test outputs 0 bits on Port A, PA0-PA7, then reads Port B, PB0-PB7. If PORT B = 255, binary 11111111, the Keyboard Test displays 'OPEN', indicating no keys on the keyboard are depressed. If PORT B ≠ 255, binary 11111111, the Keyboard Test displays 'BAD', indicating a 0 bit was detected on Port B.

If the Keyboard Test displays 'BAD' or 'OPEN' with the keyboard connector PCB in place, it usually indicates a defective 6526 CIA, U1. If the Keyboard Test displays 'BAD' with the keyboard connector PCB off, it usually indicates a shorted or depressed key on the keyboard.

MAKE SURE THE SHIFT-LOCK KEY IS NOT LOCKED IN THE CLOSED POSITION.

If an error occurs during the Keyboard Test and the keyboard has been determined good, the 6526 CIA, U1, should be replaced even though it may not be displayed as 'BAD'. If this does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

1.6.11 CONTROL PORT TEST

The Control Port Test checks both control ports, (Joystick/Paddle Ports), by outputting signals on control port 1, JOYA0-JOYA3, then reading control port 2, JOYB0-JOYB3. The paddle inputs of both control ports, POTX-POTY, are tied to +5 VDC through 110K pull-up resistors, located on the User Port Hardware Adapter.

The Control Port Test checks the paddle inputs first. The 6581 SID IC, U5, converts the analog signal, developed across the 110K resistors, to a digital output. If this digital output falls within a specified range, the Control Port Test continues.

The Control Port Test checks the joystick and push-button inputs by outputting 0 bits on Port A, PA0-PA4, and reading the input on Port B, PB0-PB4. If PORT B INPUT = PORT A OUTPUT, the control port is 'OK'. If PORT B INPUT ≠ PORT A OUTPUT, the control port is 'BAD'.

If the Control Port Test sees only 1 paddle input 'BAD' it usually indicates a defective 4066 CMOS switch, U2, or 6526 CIA, U1. If both paddle inputs are detected 'BAD', it usually indicates a defective 6581 SID IC, U5, 4066 CMOS switch, U2, or 6526 CIA, U1.

If a failure occurs during the Control Port Test, any indicated IC should be replaced. If this does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

1.6.12 SERIAL PORT TEST

The Serial Port Test performs 4 different tests on the serial port.

1) The port is set up to WRITE, (CIA1), WITHOUT setting the interrupt bit. Data is output and the data port (CIA2) is checked to see if data is waiting. If so, the Serial Port Test continues.

2) The port is set up to READ WITHOUT setting the interrupt bit. Data is output and the data wait bit is checked to see if it has been set. If so, the Serial Port Test continues.

3) The port is set up to WRITE, (CIA1), WITH the interrupt bit set. Data is output and the data port, (CIA2), is checked to see if data is waiting. If so, the Serial Port Test continues.

4) The port is set up to READ WITH the interrupt bit set. Data is output and the data wait bit is checked to see if it has been set. If so, the Serial Port is 'OK'. If any test fails, the Serial Port is 'BAD'.

During the Serial Port Test, the following rules apply:

1) If the 6526 CIA, U1, fails to clear the serial port interrupt flag, it is assumed 'BAD' and will be flagged.

2) If Data Sent was not received or Data Read was not sent, the 6526 CIA, U4, is assumed 'BAD' and will be flagged.

If a failure occurs during the Serial Port Test, any indicated IC should be replaced. If this does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

> ON THE ORIGINAL C128 PCB (REV. 6) THE SERIAL PORT, CASSETTE PORT AND IC U1 WILL ALWAYS DISPLAY 'BAD'. THIS IS DUE TO A 7407 TTL BUFFER, PCB LOCATION U60, WHICH WAS ADDED TO ALL PCB'S REV. 7 AND ABOVE.

1.6.13 USER PORT TEST

The User Port Test checks the C128 user port by generating an output signal on PA3, ATN OUT, of the 6526 CIA, U4, and reading the input on PA2. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the User Port Test continues.

A binary count is output on PB0-PB3 of the 6526 CIA, U4, and read on PB4-PB7. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the User Port Test continues.

An output signal is generated on PC2 and read on FLAG 2. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the User Port Test continues.

An output signal is generated on SP1 and read on SP2. If DATA IN ≠ DATA OUT, the user port is 'BAD'. If DATA IN = DATA OUT, the User Port Test continues.

An output signal is generated on SP2 and read on SP1. IF DATA IN = DATA OUT, the user port is 'OK'. If DATA IN ≠ DATA OUT, the user port is 'BAD'.

If a failure occurs during the User Port Test, any indicated IC should be replaced. If this does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

1.6.14 TIMER 1-A/1-B — TIMER 2-A/2-B TESTS

The Timer Tests check the internal clocks of the 6526 CIA's, U1 and U4, by setting up the timer pointers and 6526 CIA addresses to be utilized. The timers are set to run at 60 HZ, derived from the TOD, Time Of Day, inputs on pin 19 of the 6526 CIA's, U1 and U4. The timers continue to run until the interrupts are sensed. If the interrupts are sensed within 94000 clock cycles, the timers are 'OK'. If the interrupts are fast, slow or not sensed, the timers are 'BAD'.

If a failure occurs during either Timer Test, observe the status of the Interrupt Test and replace the IC indicated by the following chart:

Timer 1 A/B	Timer 2 A/B	Interrupt	8502 (U6)	6526 (U1)	6526 (U4)
OK	OK	OK	OK	OK	OK
BAD	OK	OK	OK	BAD	OK
OK	BAD	OK	OK	OK	BAD
OK	OK	BAD	BAD	OK	OK
BAD	BAD	BAD	BAD	OK	OK

If this does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Dislayed.

1.6.15 INTERRUPT TEST

The Interrupt Test checks the internal timers of the 6526 CIA's, U1 and U4, using the IRQ and NMI vectors. If an interrupt is not sensed on the IRQ of the 6526 CIA, U1, or the NMI of the 6526 CIA, U4, the interrupt is 'BAD'. If both interrupts are sensed, the Interrupt Test continues.

The internal alarms of the 6526 CIA's, U1 and U4, are tested by adding 2 seconds to the clock and waiting for the alarm to go off. If the alarm interrupt is not sensed, the interrupt is 'BAD'. If the alarm interrupt is sensed, the Interrupt Test continues.

The data line interrupt is tested by outputting data from the 6526 CIA, U1, and waiting for an interrupt to occur on the 6526 CIA, U4. Data is then output on the 6526 CIA, U4, and a check is done for an interrupt to occur on the 6526 CIA, U1. If the interrupts are sensed, the interrupt is 'OK'. If the interrupts are not sensed, the interrupt is 'BAD'.

If an error occurs during the Interrupt Test, refer to the chart in Section 1.7.14. If replacing the indicated IC does not correct the problem, refer to C128 System Diagnostic Symptoms — Section 3.1 — Diagnostic Errors Displayed.

1.6.16 SOUND TEST

The Sound Test is an audible test ONLY and no 'OK' or 'BAD' messages will be displayed. The Sound Test should produce 3 distinctive voices at 3 volume levels followed by 3 bursts of noise.

If any of the voices, volume levels or noise bursts are missing or distorted, it probably indicates a defective 6581 SID IC, U5. If replacement of the SID IC does not correct the problem, troubleshooting of the audio output circuitry will be necessary.

1.6.17 LOWER SCREEN DISPLAY

During run time, the diagnostic displays the number of cycles completed, (Count), in the bottom left hand corner of the screen.

In the bottom right hand corner of the screen, two clocks are displayed. The AM clock corresponds to the internal Time-Of-Day clock of the 6526 CIA, U1, and the PM clock corresponds to the internal Time-Of-Day clock of the 6526 CIA, U4.

The AM and PM clocks should display the EXACT SAME TIME during diagnostic run time and increment as the diagnostic tests are executing. The increments of the clocks are as follows:

Current Test	AM Clock	PM Clock	Current Test	AM Clock	PM Clock
Zero Page	00:00:00	00:00:00	Cassette	00:02:06	00:02:06
Stack Page	00:00:00	00:00:00	Keyboard	00:02:06	00:02:06
Screen Ram	00:00:00	00:00:00	Serial Port	00:02:06	00:02:06
Color Ram	00:00:11	00:00:11	Control Port	00:02:06	00:02:06
Hi Ram Bank 0	00:00:22	00:00:22	User Port	00:02:06	00:02:06
Hi Ram Bank 1	00:00:59	00:00:59	Timer 1 A	00:02:06	00:02:06
Lo Ram Bank 0	00:01:35	00:01:35	Timer 1 B	00:02:06	00:02:06
Lo Ram Bank 1	00:02:06	00:02:06	Timer 2 A	00:02:06	00:02:06
Kernal ROM	00:02:06	00:02:06	Timer 2 B	00:02:06	00:02:06
Basic Lo ROM	00:02:06	00:02:06	Interrupt	00:02:40	00:02:40
Basic Hi ROM	00:02:06	00:02:06	Alarm Set*	00:02:42	00:02:42
Character ROM	00:02:06	00:02:06	Sound Test	00:02:44	00:02:44
PLA Test	00:02:06	00:02:06	New Cylce**	00:02:56	00:02:56

* = Alarm set does not display on the screen
** = Beginning of the second cycle

FAILURE MODES:

Incorrect AM Clock — Possible 6526 CIA, U1, Failure
Incorrect PM Clock — Possible 6526 CIA, U4, Failure
Incorrect Both Clocks — Possible 60HZ TOD Input Failure

C128 SYSTEM TROUBLESHOOTING

2.1 BASIC PRELIMINARY CHECKS

There are a few basic checks which must be made on the C128 when troubleshooting a SYSTEM THAT DISPLAYS NO VIDEO ON POWER UP IN EITHER 40 OR 80 COLUMN MODE. There are several things which may cause this symptom but these BASIC SIGNALS MUST BE PRESENT in order for the system to operate. If all of these Basic Areas seem correct, more Advanced Checks are covered in SECTIONS 2.6 thru 2.15. All signals are taken with the diagnostic cartridge installed and power applied to the system unless specified. A **P** preceding the step number indicates signals which must be measured as power is applied to the system.

ALL SIGNALS ARE TAKEN WITH THE DIAGNOSTIC CARTRIDGE INSTALLED
ALL MEASUREMENTS ARE WITHIN A ±10% TOLERANCE
ALL READINGS ARE TAKEN WITH AN OSCILLOSCOPE

P INDICATES SIGNALS WHICH MUST BE MEASURED ON SYSTEM POWER UP

SOMETIMES USING THE RESET SWITCH WILL BOOT THE DIAGNOSTIC IF NORMAL POWER UP DOES NOT PRODUCE CORRECT SCREEN DISPLAY

STEP 1 Measure the voltage on pin 25 (+5VDC) of the 6581 SID - U5.
- Result = +5 VDC Level - Continue to Step 2

STEP 2 Measure the signal on pin 28 (+12VDC) of the 6581 SID - U5.
- Result = +12 VDC Level - Continue to Step 3

If any result is incorrect, Refer to Section 2.2 - SYSTEM POWER SUPPLY

(P) STEP 3 Measure the signal on pin 40 (RESET) of the 8502 MPU - U6.
- Result = 0 VDC on System Power Up w/+5 VDC in 1 Second - Continue to Step 4

If the result is incorrect, Refer to Section 2.3 - SYSTEM RESET

STEP 4 Measure the signal on pin 29 (PHI COLOR) of the 8564 VIC - U21.
- Result = 14.3 MHZ Clock - Continue to Step 5

STEP 5 Measure the signal on pin 30 (PHI IN) of the 8564 VIC - U21.
- Result = 8.18 MHZ Clock - Continue to Step 6

STEP 6 Measure the signal on pin 18 (1 MHZ) of the 8564 VIC - U21
- Result = 1 MHZ Clock - Continue to Step 7

STEP 7 Measure the signal on pin 23 (2 MHZ) of 8564 VIC - U21.
- Result = 2 MHZ Clock - Continue to Step 8

STEP 8 Measure the signal on pin 25 (Z80 PHI) of 8564 VIC - U21.
- Result = 4 MHZ Clock - Continue to Step 9

STEP 9 Measure the signal on pin 2 (DCLK) of 8564 VDC - U22.
- Result = 16 MHZ Clock - Continue to Step 10

If any signal is incorrect, Refer to Section 2.4 - SYSTEM CLOCKS

STEP 10 Measure the signal on pin 16 (CHROMA) of 8564 VIC - U21.
- Result = .5-1 V CHROMA Signal Riding On A 2-3 V Level - Continue to Step 11

STEP 11 Measure the signal on pin 17 (SYNC/LUM) of 8564 VIC - U21.
- Result = 4-5 V Composite Signal - Continue to Section 2.6

If any result is incorrect, Refer to Section 2.5 - SYSTEM VIDEO

ALL THE SIGNALS LISTED, STEP 1 THROUGH STEP 11, MUST BE PRESENT FOR THE SYSTEM TO PRODUCE THE CORRECT VIDEO DISPLAY IF ALL SIGNALS SEEM TO BE CORRECT, BEGIN THE STEPS LISTED IN SECTIONS 2.6 THRU 2.7 - TROUBLESHOOTING THE 4164 SYSTEM RAM

2.2 TROUBLESHOOTING THE C128 SYSTEM POWER SUPPLY

By referring to this section, it is assumed that either the +5 VDC, +12 VDC or both measurements from BASIC PRELIMINARY CHECKS, STEPS 1 thru 2 are incorrect.

2.2.1 DEFECTIVE +5 VDC SUPPLY

STEP 1 Measure the voltage on the (+ LEG) of Capacitor - C107.
- Result = +5 VDC Level - No +5 VDC Problem Open +5 VDC Trace
- Result = Incorrect - Continue to Step 2

STEP 2 Measure the voltage on the (+ LEG) of Capacitor - C99.
- Result = +5 VDC Level - Defective Switch - S1
- Result = Incorrect - Continue to Step 3

STEP 3 Measure the voltage on pin 1 (+5 IN) of Connector CN11.
- Result = +5 VDC Level - Defective Filter - L5
- Result = Incorrect - Defective Power Supply

2.2.2 DEFECTIVE +12 VDC SUPPLY

STEP 1 Measure the voltage on the (+ LEG) of Capacitor - C111.

- Result = +12 VDC Level - No +12 VDC Problem Open +12 VDC Trace
- Result = Incorrect - Continue to Step 2

STEP 2 Measure the voltage on the Anode of Diode - CR10

- Result = +18 VDC Level - Unregulated - Defective Regulator - U59
- Result = Incorrect - Continue to Step 3

STEP 3 Measure the voltages on the AC Inputs of Rectifier CR13.

- Result = 9 VAC On Both Inputs - Continue to Step 4
- Result = Incorrect 9 VAC1 - Continue to Step 3.1
- Result = Incorrect 9 VAC2 - Continue to Step 3.3

STEP 3.1 Measure the voltage on (+ LEG) of Capacitor - C97

- Result = 9 VAC - Defective Switch - SW1
- Result = Incorrect - Continue to Step 3.2

STEP 3.2 Measure the voltage on pin 3 of Capacitor CN11.

- Result = 9 VAC - Defective Switch - L5
- Result = Incorrect - Defective Power Supply

STEP 3.3 Measure the voltage on pin 5 of Connector - CN11.

- Result = 9 VAC - Defective Filter L5
- Result = Incorrect - Defective Power Supply

STEP 4 Measure the voltage on the Anode of Diode - CR11.

- Result = 9 VAC riding on 9 VDC Level - Defective CR10
- Result = 0 VDC - Defective CR10
- Result = 9 VDC Only - Defective CR11
- Result = 9 VAC Only - Defective CR13

2.3 TROUBLESHOOTING THE C128 SYSTEM RESET

By referring to this section it is assumed that the RESET SIGNAL FROM BASIC PRELIMINARY CHECKS, STEP 3 is incorrect.

(P) STEP 1 Measure the signal on pin 8 of IC - U63.

- Result = 0 V to 5 V Level in about 1 second - No Reset Problem Open Reset Trace
- Result = Incorrect - Continue to Step 2

(P) STEP 2 Measure the signal on pin 9 of IC - U63.

- Result = 5 V on system power to 0 V in about 1 second - Defective U63
- Result = Incorrect - Continue to Step 3

(P) STEP 3 Measure the signal on pin 8 of IC - U63.

- Result = slow rise from 0 V to +5 V - Continue to Step 4
- Result = Incorrect - Defective CR15, C91, U63

(P) STEP 4 Measure the signal on pin 12 of IC - U63.

- Result = slow rise from 0 V to +5 V then quick drop to 0 V - Defective U63
- Result = Incorrect - Defective CR16, C92, U63

2.4 TROUBLESHOOTING THE C128 SYSTEM CLOCKS

By referring to this section it is assumed that one or more of the system clock signals from BASIC PRELIMINARY CHECKS 4 thru 9 are incorrect.

2.4.1 INCORRECT 14.3 MHZ CLOCK

STEP 1 Measure the signal on pin 13 of 7701/8701 - U28.

- Result = 14.3 MHZ Clock - Defective U28,U21
- Result = Incorrect - Adjust C20 Defective Y2, U28

2.4.2 INCORRECT 8.18 MHZ CLOCK

STEP 1 Measure the signal on pin 13 of 7701/8701 - U28.

- Result = 14.3 MHZ Clock - Defective U28, U21, U29
- Result = Incorrect - Adjust C20 Defective Y2, U28

2.4.3 INCORRECT 1.0 MHZ CLOCK

STEP 1 Measure the signals on pins 6, 8 of 7701/8701 - U28.

- Result = Pin 6, 8.18 MHZ Clock Pin 8, 14.3 MHZ Clock - Defective U21, U56, U12 U5, U3

SPECIAL NOTE: U3 is valid only for some of the original PCBs. On the newer PCBs pin 6 of IC U3 will be tied to +5 VDC.

2.4.4 INCORRECT 2.0 MHZ CLOCK

STEP 1 Measure the signal on pins 6, 8 of 7701/8701 - U28.

- Result = Pin 6, 8.18 MHZ Clock
  Pin 8, 14.3 MHZ Clock - Defective U21, U6, U7

2.4.5 INCORRECT 4.0 MHZ CLOCK

STEP 1 Measure the signals on pins 6, 8 of 7701/8701 - U28.

- Result = Pin 6, 8.18 MHZ Clock
  Pin 8, 14.3 MHZ Clock - Continue to Step 2

STEP 2 Measure the signal on pin 25 of 8564 VIC - U21.

- Result = 4.0 MHZ Clock - Continue to Step 3
- Result = Incorrect - Defective U21, U60

STEP 3 Measure the signals on pins 10, 12 of 7407 - U60.

- Result = 4.0 MHZ Clock - Defective Q6
- Result = Incorrect - Defective U60, Q6

2.4.6 INCORRECT 16 MHZ CLOCK

STEP 1 Measure the signal on pin 8 of Crystal - Y1.

- Result = 16 MHZ Clock - Open Trace to U22
- Result = Incorrect - Defective U22, Y1

2.5 TROUBLESHOOTING THE C128 SYSTEM VIDEO

(P) STEP 1 Measure the signal on pin 13 (VIC) of 8564 VIC - U21.

- Result = 4-5 V with Negative Pulses
  One Time On Reset - Continue to Step 2
- Result = Incorrect - Defective U11, U21

SPECIAL NOTE: The VIC Input depends on the VIC Output of the PLA and all associated circuitry being correct.

See Troubleshooting the 8721 PLA - Section 2.13

STEP 2 Measure the signal on pin 14 R/W of 8564 VIC - U21.

- Result = 4-5 V with Negative Pulses - Continue to Step 3
- Result = Incorrect - Defective U21, U57, U5, U1, U4

SPECIAL NOTE: The R/W Input depends on the R/W Output of the MOS 8502, AEC Output of VIC, Q Output of IC U56, +5 VDC DMA and all associated circuitry being correct.

See Troubleshooting the MOS 8502 Microprocessor - Section 2.9

See Troubleshooting the 8564 VIC - Section 2.12

STEP 3 Measure the signal on pin 16 (CHROMA) of 8564 VIC - U21.

- Result = .5-1 V Chroma on a 2-3 V Level - Continue to Step 4
- Result = Incorrect - Defective U21, M1

STEP 4 Measure the signal on pin 17 (SYNC/LUM) of 8564 VIC - U21.

- Result = 4-5 V Composite - Continue to Step 5
- Result = Incorrect - Defective U21, M1

STEP 5 Measure the signal on pin 5 (COMPOSITE) of Connector CN8.

- Result = 2-3 V Composite - Continue to Step 6
- Result = Incorrect - Defective M1

STEP 6 Measure the signal on pin 6 (LUMINANCE) of Connector CN8.

- Result = 1-2 V Sync/Lum - Continue to Step 7
- Result = Incorrect - Defective M1

STEP 7 Measure the signal on pin 7 (CHROMA) of Connector CN8.

- Result = .5-1 V Chroma - Video is OK
- Result = Incorrect - Defective M1

2.6 TROUBLESHOOTING THE 4164 SYSTEM RAM

When all of the Basic signals are present the C128 system should be capable of producing video information to the screen. In order to do this it must first be able to complete the Initial Start-up Sequence. There are many things which may keep the system from this task. The C128 must be able to access certain memory locations on power up. In order to do this, certain input signals must be present to the system RAM area. Following the steps listed should determine if the system RAM is being accessed correctly.

All SPECIAL NOTES for appropriate signals are listed and should be referenced before continuing to the next step if an incorrect signal is found.

IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

Overview Of The C128 Memory Organization

Because the C128 computer uses Dynamic RAM, a refresh cycle must occur at least every 2 milliseconds. Each RAM test in the C128 diagnostic contains a delay which allows memory to refresh. This is the time when most RAM failures occur. If any one of the RAM tests fails, the location of the first pass of BAD RAMs displayed should be observed. It is very important to do so since the diagnostic will only compound the RAM problem by further testing. (Remember, the diagnostic program needs memory too!).

Example: If the Stack Page Test displays 2 RAM ICs BAD, the indicated RAM ICs should be replaced and the diagnostic re-started. The diagnostic should never be allowed to continue testing as erroneous results will normally be displayed.

Because the 8502 MPU can only 'see' 64K of memory at one time, it is necessary to 'bank' memory in and out. The C128 has 2 banks of 64K RAM each. In order for the system to 'see' this RAM it uses the 8722 MMU, U7. The MMU is controlled by the 8721 PLA, U11. PLA or MMU failures are not easily detected by the diagnostic although failures can sometimes be determined through the OVERALL test results.

Example: Both BAD RAM patterns for BANK 0 match BANK 1 and all I/O tests fail.

STEP 1 Measure the signal on pin 4 (RAS) of 4164 RAM - U38 and U46.

- Result = Pulsing Strobe - Continue to Step 2
- Result = Incorrect - Defective U21, U38 - U53

SPECIAL NOTE: The RAS input depends on the RAS output from VIC and all associated circuitry being correct.

See Troubleshooting the 8564 VIC - Section 2.12

STEP 2 Measure the signal on pin 15 (CASO) of 4164 RAM - U38 - U45.

- Result = Pulsing Strobe - Continue to Step 3
- Result = Incorrect - Defective U9, U38 - U45

SPECIAL NOTE: The CASO input depends on the CAS output from VIC, GCASO output, (Generated from the CASO output from the MMU and the CASENB output from the PLA), and all associated circuitry being correct.

See Troubleshooting the 8564 VIC - Section 2.12
See Troubleshooting the 8722 MMU - Section 2.14
See Troubleshooting the 8721 PLA - Section 2.13

(P) STEP 3 Measure the signal on pin 15 (CAS1) of 4164 RAM - U46 - 53.

- Result = 4-5 V Level with Negative Pulses one time on Reset - Continue to Step 4
- Result = Incorrect - Defective U9, U38 - U45.

STEP 4 Measure the signals on pins 5-7, 9-13 (MA0-MA7) of 4164 - U38 - U53.

- Results = 4-5 V Pulsing Address - Continue to Step 5
- Results = Incorrect Pins 5-7, 12 (MA0-MA3) - Defective U15, RP4 U38 thru U53
- Results = Incorrect Pins 9-11, 13 (MA4-MA7) - Defective U14, RP3 U38 thru U53

SPECIAL NOTE: The MA0-MA7 Address Lines depend on A0-A7 of the System Address Bus being correct.

See Troubleshooting the System Address Bus - Section 2.11

(P) STEP 5 Measure the signals at pin 2 (D0-D7) of 4164 RAM - U38 thru U45.

- Results = Strong +5 V Data Pulses immediately when power is applied to the system - Continue to Section 2.7
- Results = Incorrect on Any Pin - Continue to Section 2.7

SPECIAL NOTE: A Data Pulse that is below +4 Volts or slow in getting to the +5 Volt level usually indicates a defective 4164 RAM.

SPECIAL NOTE: The D0-D7 Data Lines depend on D0-D7 of the System Data Bus being correct.

See Troubleshooting the System Data Bus - Section 2.10

NOTE * NOTE * NOTE * NOTE * NOTE * NOTE * NOTE * NOTE * NOTE

SOME OF THE FOLLOWING SECTIONS ARE FOR INFORMATION ONLY AND ARE NOT TO BE CONSIDERED RECOMMENDATIONS. THESE SECTIONS ARE IDENTIFIED, AND USING THE METHODS DESCRIBED MAY VOID PARTIAL OR ALL CREDIT IF THE PCB IS RETURNED TO COMMODORE BUISNESS MACHINES DAMAGED IN ANY WAY.

NOTE * NOTE * NOTE * NOTE * NOTE * NOTE * NOTE * NOTE * NOTE

SECTION 2.7 IS FOR INFORMATION ONLY AND IS NOT TO BE CONSIDERED A RECOMMENDATION. USING THIS METHOD MAY VOID PARTIAL OR ALL CREDIT IF THE PCB IS RETURNED TO COMMODORE BUSINESS MACHINES DAMAGED IN ANY WAY.

2.7 ADVANCED 4164 RAM TROUBLESHOOTING

In order for the C128 system to complete the proper power-up sequence, all of the previously listed signals must be correct. If all these signals are correct it is still possible for a defective 4164 RAM IC to keep the system from coming up. Normally if the defective RAM is in the Hi RAM bank area, U46-U53, the diagnostic will bring the system up and display the defective RAM location. To eliminate the system RAM as a possibility of keeping the system from coming up, the following steps may be followed:

1. Make sure the signals in Steps 1 thru 5 are correct.
2. Turn the power OFF to the system.
3. Cut one end of each resistor R29 and R30 and lift from the board.
4. Solder a piece of jumper wire to the lifted ends of each resistor and solder the other end to the PCB, reversing the inputs.

   Example: Jumper wire of R29 should be connected to the R30 location of the the PCB and vice versa for resistor R30.
5. Make sure the diagnostic is installed and apply power to the system.

If the diagnostic brings the system up, it is an indication of a defective 4164 RAM IC in the Lo RAM bank area, U38-U45, and the Diagnostic should display the defective RAM location.

NOTE: By reversing the CAS0 and CAS1 input signals, R29 and R30, to the system RAM, Lo Bank and Hi Bank have now also been reversed. Therefore if one of the RAM ICs is displayed 'BAD', an adjustment must be made for the location.
Example: U38 now becomes U46, U39 now becomes U47, etc.

If the diagnostic still does not bring up the system, the 4164 RAM is probably good, and the steps in Section 2.8 should be implemented.

2.8 TROUBLESHOOTING THE Z80 MIROPROCESSOR

Because the C128 must power up with the Z80 as the master processor, this is the next step when troubleshooting a system which displays 'No Video' on either 40 or 80 column screens.

All SPECIAL NOTES for appropriate signals are listed and should be referenced before continuing to the next step if an incorrect signal is found.

> IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

STEP 1 Measure the CLOCK signal on pin 6 (PHI IN) of Z80 - U10.

- Result = 4 MHZ Clock - 5-6V - Continue to Step 2
- Result = Incorrect - Defective Q6, U60, U10

SPECIAL NOTE: For the PHI IN Clock input to be correct, the Z80 PHI output from VIC and all associated circuitry must be correct.

See Basic Preliminary Checks - Section 2.1 - Step 8

(P) STEP 2 Measure the signals on pins 20 (Z80 I/O, 27 (M1), 22 (WR) of Z80 - U10.

- Result = 4-5 V Level With Negative Pulses One Time On Reset - Continue to Step 3
- Result = Incorrect pin 20 (Z80 I/O) - Defective U11, U10
- Result = Incorrect pin 27 (MI) - Defective U10, U31
- Result = Incorrect pin 22 (WR) - Defective U10, U31

(P) STEP 3 Measure the signals on pin 25 (BUSRQST), 23 (BUSACK) of Z80 - U10.

- Result = 4-5 V to 0 V on Reset - Continue to Step 4
- Result = Incorrect pin 25 (BUSRQST) - Defective U60, U37, U10

SPECIAL NOTE: For the BUSRQST input to be correct, the BA and AEC outputs from VIC, Z80EN output from the MMU, BUSACK output from Z80 and all associated circuitry must be correct.

See Troubleshooting the 8564 VIC — Section 2.6

See Troubleshooting the 8722 MMU — Section 2.14

See Result Pin 23 (BUSACK) Step 3

- Result = Incorrect pin 23 (BUSACK) - Defective U37, U10

(P) STEP 4 Measure the signal on pin 21 (RD) of Z80 - U10.

- Result = 4-5 V Level with Negative Pulses One Time on Reset to 1.5-2.5 V Level - Continue to Step 5
- Result = Incorrect - Defective U12

(P) STEP 5 Measure the signals on pins 7-10, 12-15 (ZD0-ZD7) of Z80 - U10.

- Result = 4-5 V Pulses on 1.5-2.5 V Level One Time on Reset - Continue to Section 2.9
- Result = Incorrect - Defective U12, U13, U10

2.9 TROUBLESHOOTING THE MOS 8502 MICROPROCESSOR

If all the Z80 signals seen correct, the Z80 has powered up and the MOS 8502 must take control of the system. The MOS 8502 microprocessor is the next step in troubleshooting a system which displays 'No Video' on either 40 or 80 column screens.

All SPECIAL NOTES for appropriate signals are listed and should be referenced before continuing to the next step if an incorrect signal is found.

IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

STEP 1 Measure the signals on pins 2 (UBA), 39 (R/W) of 8502 - U6.

- Result = 4-5 V Level With Negative Pulses - Continue to Step 2
- Result = Incorrect pin 2 (UBA) - Defective U6, U61

SPECIAL NOTE: For the UBA input to be correct, the BA and AEC outputs from VIC, Z80EN output from the MMU and all associated circuitry must be correct.

See Troubleshooting the 8564 VIC - Section 2.12
See Troubleshooting the 8722 MMU - Section 2.14

- Result = Incorrect pin 39 (R/W) - Defective U6, U8

(P) STEP 2 Measure the signal on pin 5 (AEC) of 8502 - U6.

- Result = 0 to 4-5 V Level on Reset - Continue to Step 3
- Result = Incorrect - Defective U6, U61

SPECIAL NOTE: For the AEC input to be correct the BUSACK output from the Z80, the +5 VDC DMA output from the cartridge port and all associated circuitry must be correct.

See Troubleshooting the Z80 Microprocessor - Section 2.8

STEP 3 Measure the signals on pins 31-38 (D0-D7) of 8502 - U6.

- Result = 4-5 V Pulsing Data - Continue to Step 4
- Result = Incorrect - Defective U6, U21, U22, U7, U32, U33, U34, U35, U5, U12, U13, U18, U20, U1, U4, U36

SPECIAL NOTE: If only one data line is incorrect the system ram must be verified before any of the defective ICs listed can be considered valid.

See Troubleshooting the 4164 System RAM - Sections 2.6 - 2.7

SPECIAL NOTE: If several or all of the data lines are incorrect, it will be necessary to troubleshoot the system data bus.

See Troubleshooting the System Data Bus - Section 2.10

SPECIAL NOTE: If any of the address lines are incorrect, troubleshooting of the system address bus will be necessary.

See Troubleshooting the System Address Bus - Section 2.11

SPECIAL NOTE: U36 listed as a possible defective IC is valid only if an IC is installed in that location.

STEP 4 Measure the signals on pins 7-20 (A0-A13), 22-23 (A14-A15) of 8502 - U6.

- Result = 4-5 V Pulsing Address - Continue to Step 5
- Result = Incorrect pin 7 (A0) - Defective U6, U10, U5, U7, U15, U55, U32, U33, U34, U35, U1, U4, U22, RP9, U36
- Result = Incorrect pins 8-10 (A1-A3) - Defective U6, U10, U5, U7, U15, U55, U32, U33, U34, U35, U1, U4, RP9, U36
- Result = Incorrect pin 11 (A4) - Defective U6, U10, U5, U54, U14, U55, U32, U33, U34, U35, RP9, U36
- Result = Incorrect pins 12-14 (A5-A7) - Defective U6, U10, U54, U14, U55, U32, U33, U34, U35, RP9, U36
- Result = Incorrect pins 15-16 (A8-A9) - Defective U6, U10, U7, U32, U33, U34, U35, U3, U62, U36, RP10
- Result = Incorrect pin 17 (A10) - Defective U6, U10, U7, U11, U32, U33, U34, U35, U31, U62, RP10, U36
- Result = Incorrect pin 18 (A11) - Defective U6, U10, U7, U11, U32, U33, U34, U35, U3, U62, RP10, U36
- Result = Incorrect pin 19 (A12) - Defective U6, U10, U7, U11, U33, U34, U62, RP10, U36
- Result = Incorrect pin 20 (A13) - Defective U10, U6, U7, U11, U8, U33, U34, U35, U62, RP10, U36
- Result = Incorrect pin 22 (A14) - Defective U10, U6, U7
- Result = Incorrect pin 23 (A15) - Defective U6, U10, U7, U11, U62, RP10, U36

NOTE * NOTE * NOTE * NOTE * NOTE* NOTE * NOTE * NOTE
SECTIONS 2.10 AND 2.11 ARE FOR INFORMATION ONLY AND ARE NOT TO BE CONSIDERED A RECOMMENDATION. USING THESE METHODS MAY VOID PARTIAL OR ALL CREDIT IF THE PCB IS RETURNED TO COMMODORE BUSINESS MACHINES DAMAGED IN ANY WAY.

2.10 ADVANCED TROUBLESHOOTING OF THE SYSTEM DATA BUS

Normally, an incorrect data line will be held in either a high or a low condition. The IC which is causing this problem can usually be isolated quite easily by implementing the following steps:

NOTE: Any pins which must be cut should be cut next to the PCB to allow resoldering, if necessary.

1) Make sure power is OFF to the system before attempting these procedures.
2) Replace any socketed IC associated with the incorrect data line one at a time and retest after each replacement.
3) Cut and lift the +5 VDC supply pin of one of the associated ICs, measure the incorrect data line on an IC other than the one with the pin lifted.
4) If the data line is correct it indicates the IC with the cut pin is defective and must be replaced.
5) If the data line is still incorrect, turn power OFF, and resolder the lifted pin.
6) Continue with step 3 through step 5 until the correct data line is displayed.

2.11 ADVANCED TROUBLESHOOTING OF SYSTEM ADDRESS BUS

Normally an incorrect address line will be held in either a high or low condition. The IC which is causing the problem can usually be isolated quite easily by implementing the following steps:

NOTE: Any pins which must be cut should be cut next to the PCB to allow resoldering, if necessary.

1) Make sure power is OFF to the system.
2) Replace any socketed IC associated with the incorrect address line one at a time and retest after each replacement.
3) Cut and lift the pin on the MOS 8502 which corresponds to the incorrect signal and measure the signal on the lifted pin.
4) If the signal is not correct, replace the MOS 8502.
5) If the signal on the lifted pin is correct, turn power OFF, and resolder the lifted pin.
6) Cut and lift the pin of the associated ICs which correspond to the incorrect signal, one at a time, and measure for the correct signal on the MOS 8502.
7) If the address line is correct, replace the IC with the lifted pin.
8) If the address line is still incorrect, turn power OFF, and resolder the lifted pin.
9) Continue with step 6 thru step 8 until the correct address line is displayed.

STEP 4 Measure the signals on pins 32-37 (VMA0-VMA5), 38-39 (VA6-VA7) of the 8564 VIC - U21.

- Result = 4-5 V Pulsing Address - Continue to Step 5
- Result = Incorrect pins 32-35 (VMA0-VMA3) - Defective U21, U15, U17
- Result = Incorrect pins 36-37 (VMA4-VMA5) - Defective U21, U14, U17, U11
- Result = Incorrect pins 38-39 (VA6-VA7) - Defective U21, U26, U17

STEP 5 Measure the signals on pins 43-46 (D8-D11) of 8564 VIC- U21.

- Result = 4-5 V Pulsing Data - Continue to Section 2.13
- Result = Incorrect - Defective U21, U19

2.13 TROUBLESHOOTING THE 8721 PROGRAMMABLE LOGIC ARRAY (PLA)

If all the 8564 VIC signals seem correct, the VIC should be selected and able to produce video information. Because the PLA is responsible for generating chip selects to the system ROM and 8564 VIC, along with write enable strobes to both color RAM and DRAM and also selects the diagnostic cartrdige, it is the next step when troubleshooting a system which produces 'No Video' to either 40 or 80 column screens.

All SPECIAL NOTES for appropriate signals are listed and should be referenced before continuing to the next step if an incorrect signal is found.

IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

STEP 1 Measure the signal on pin 9 (AEC) of 8721 PLA - U11.

- Result = 4-5 V Strobe - Continue to Step 2
- Result = Incorrect - Defective U11, U21, U29, U61, U26, U20, U17

SPECIAL NOTE: The AEC input depends on the AEC output from VIC and all associated circuitry being correct.

See Troubleshooting the 8564 VIC - Section 2.12

(P) STEP 2 Measure the signal on pin 13 (BUSACK) of 8721 PLA - U11.

- Result = 0 V to +5 V on Reset - Continue to Step 3
- Result = Incorrect - Defective U11, U8, U37, U61

SPECIAL NOTE: The BUSACK input depends on the BUSACK output from Z80 and all associated circuitry being correct.

See Troubleshooting the Z80 Microprocessor - Section 2.8

STEP 3 Measure the signals on pins 19 (VMA4), 20 (VMA5) of 8721 PLA - U11.

- Result = 4-5 V Pulsing Address - Continue to Step 4
- Result = Incorrect - Defective U11, U21, U14, U17

STEP 4 Measure the signal on pin 21 (BA) of 8721 PLA - U11.

- Result = 3-4 V Level with Negative Pulses - Continue to Step 5
- Result = Incorrect - Defective U11, U21, U60, U61, U63

SPECIAL NOTE: The BA input depends on the BA output from VIC and all associated circuitry being correct.

See Troubleshooting the 8564 VIC - Section 2.12

STEP 5 Measure the signal on pin 30 (ROML) of 8721 PLA - U11.

- Result = 3-4 V Pulses - Continue to Step 6
- Result = Incorrect - Defective U11 Diagnostic Cartridge

(P) STEP 6 Measure the signal on pin 34 (ROM4) of 8721 PLA - U11.

- Result = 3-4 V Pulses to 3-4 V Level on Diagnostic Initialization - Continue to Step 7
- Result = Incorrect - Defective U11, U35

(P) STEP 7 Measure the signal on pin 35 (ROM3), 36 (ROM2) of 8721 PLA - U11.

- Result = 3-4 V Level with Negative Pulses one time until Diagnostic Initialization - Continue to Step 8
- Result = Incorrect pin 35 (ROM3) - Defective U11, U34
- Result = Incorrect pin 36 (ROM2) - Defective U11, U33

(P) STEP 8 Measure the signals on pins 37 (ROM1) of 8721 PLA - U11.

- Result = 4-5 V Level with a 1-2 V Negative Pulse until Reset - Continue to Step 9
- Result = Incorrect - Defective U11, U32

(P) STEP 9 Measure the signals on pins 38 (IOCS), 40 (DWE) of 8721 PLA - U11.

- Result = 4-5 V Level with Negative Pulses until Diagnostic Initialization - Continue to Step 10
- Result = Incorrect pin 38 (IOCS) - Defective U11, U21
- Result = Incorrect pin 40 (DWE) - Defective U11, U38 thru U53

SPECIAL NOTE: U38 thru U53 are not valid until System RAM has been verified.

See Troubleshooting the 4164 System RAM - Sections 2.6 — 2.7

STEP 5 Measure the signals on pins 7-10 (TA11/MA11-TA8/MA8) of MMU - U7.

- Result = 4-5 V Pulsing Address - Continue to Step 6
- Result = Incorrect pins 7-8 (TA11, TA10) - Defective U7, U15, U21, U18, U62
- Result = Incorrect pins 9-10 (TA9, TA8) - Defective U7, U15, U21, U18, U19, U62

STEP 6 Measure the signal on pin 16 (GAEC), 12 (CAS0) of 8722 MMU - U7.

- Result = 3-4 V Strobe - Continue to Step 7
- Result = Incorrect pin 16 (GAEC) - Defective U7, U61

SPECIAL NOTE: For the GAEC input to be correct the AEC output from VIC, the +5 VDC DMA from the expansion port and all associated circuitry must be correct.

See Troubleshooting the 8564 VIC — Section 2.12

STEP 7 Measure the signal on pin 43 (Z80EN) of 8722 MMU - U7.

- Result = 0 to +5 V on Reset - Continue to Section 2.15
- Result = Incorrect - Defective U7, U61, U37

2.15 SELECTING THE 8563 — 80 COLUMN VIDEO DISPLAY CONTROLLER (VDC) AND 6526 COMPLEX INTERFACE ADAPTER (CIA) CHIPS

Although the 8563 VDC is used primarily for the 80 column display and normally does not affect the 40 column mode and the 6526 CIAs used primarily for periphial interfacing, they must be selected for the system to produce video information. The final step in troubleshooting a system which produces 'No Video' on either 40 or 80 column screens is the chip selects of the 8563 VDC and 6526 CIAs.

> IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

(P) STEP 1 Measure the signal on pin 7 (CS8563) of 8563 Controller - U22.

- Result = 4-5 V Level with Negative Pulses until Diagnostic Initialization - Continue to Step 2
- Result = Incorrect - Defective U3, U22

STEP 2 Measure the signal on pin 23 (CIA1) of 6526 - U1.

- Result = 4-5 V with Negative Pulses - Continue to Step 3
- Result = Incorrect - Defective U3, U1

STEP 3 Measure the signal on pin 23 (CIA2) of 6526 - U4.

- Result = 4-5 V Level - Continue to Step 4
- Result = Incorrect - Defective U3, U4

STEP 4 PCB REPLACEMENT

Although the steps listed in Section 2.1 thru Section 2.15 should cover 90% of C128 systems which display 'No Video' on powerup, there may be other less noticeable problems which may cause this same symptom. Because these problems may take a great amount of time to find, BOARD REPLACEMENT at this point is recommended.

SECTION 3

C128 SYSTEM DIAGNOSTIC SYMPTOMS

3.1 DIAGNOSTIC ERRORS DISPLAYED

When the C128 diagnostic runs through the tests, several decisions must be made by the software before any IC is displayed 'BAD'. Normally the decisions are correct and the IC displayed is truly defective. Sometimes a defective IC may make another one look bad which causes the diagnostic to make a wrong decision and display a good IC or more than one ICs defective.

Normally, if only one IC is displayed defective, the IC should be replaced and the diagnostic test run again. If the IC is still displayed 'BAD' or more than one IC is flagged at the start, the troubleshooting charts that follow should help determine the true defective IC.

C128 System Diagnostic Symptoms (Continued)

ERRORS IN THESE CHARTS ARE DISPLAYED WITHOUT THE KEYBOARD PCB CONNECTOR INSTALLED

CASS PORT	KBRD TEST	CNTRL PORT	SER PORT	USER PORT	TMR1 A/B	TMR2 A/B	INT TEST	AM CLK	PM CLK	BAD IC DISPLAY	CHECK SIGNAL	ON IC
OK	OPEN	BAD	OK	OK	OK	OK	OK	OK	OK	U1 U20	PB0-4 PA6-7 LP	6526 CIA-U1 6526 CIA-U1 8563 VDC-22
OK	BAD	OK	OK	OK	OK	OK	OK	OK	OK	U1	PB0-6 LP	6526 CIA-U1 8563 VDC-U22
OK	OPEN	OK	OK	OK	OK	OK	BAD	BAD	BAD	U1 U4	TOD TOD	6526 CIA-U1 6526 CIA-U4
BAD	OPEN	BAD	BAD	OK	BAD	OK	BAD	BAD	OK	U1,U4, U5	CIA1	6526 CIA-U1
BAD	OPEN	OK	BAD	OK	OK	OK	OK	OK	OK	U1 U1,U4	FLAG PA5-7 FSDIR	6526 CIA-U1 6526 CIA-U4 8722 MMU-U7
OK	OPEN	OK	OK	BAD	OK	OK	OK	OK	OK	U4	PB0-7 PA3	6526 CIA-U4 6526 CIA-U4
OK	OPEN	OK	OK	OK	OK	OK	BAD	OK	BAD	U4	TOD	6526 CIA-U4
BAD	OPEN	OK	BAD	BAD	OK	BAD	BAD	OK	OK	U1,U4	CIA2	6526 CIA-U4
OK	OPEN	OK	OK	BAD	OK	OK	BAD	OK	OK	U1,U4	FLAG	6526 CIA-U4
OK	OPEN	OK	BAD	BAD	OK	OK	OK	OK	OK	U4	PA2-6	6526 CIA-U4
OK	OPEN	OK	BAD	OK	OK	OK	BAD	OK	OK	U1,U4	PA7	6526 CIA-U4
BAD	OPEN	BAD	OK	OK	OK	OK	OK	OK	OK	U6,U1	MTR	8502 MPU-U6
BAD	BAD	OK	OK	OK	OK	OK	OK	OK	OK	U6,U1	MTR WRT	8502 MPU-U6 8502 MPU-U6
OK	OPEN	OK	BAD	OK	OK	OK	OK	OK	OK	U1	SENSE	8502 MPU-U6
BAD	OPEN	OK	OK	OK	OK	OK	BAD	OK	OK	U1,U4	SENSE	8502 MPU-U6
BAD	OPEN	OK	OK	OK	OK	OK	OK	OK	OK	U6	WRT	8502 MPU-U6
OK	OPEN	OK	OK	OK	OK	OK	BAD	OK	OK	U4 U1	IRQ NMI	8502 MPU-U6 8502 MPU-U6
OK	BAD	BAD	BAD	BAD	BAD	BAD	BAD	BAD	BAD	U1,U4 U5	M1	Z80 MPU-U10

ZERO PAGE	STACK PAGE	SCREEN RAM	COLOR RAM	HI RAM BANK 0	HI RAM BANK 1	LO RAM BANK 0	LO RAM BANK 1	BAD IC DISPLAY	CHECK SIGNAL	ON IC
OK	OK	OK	BAD	OK	OK	OK	OK	U41	D11	8564 VIC-U21
OK	OK	OK	BAD	OK	OK	OK	OK	U40	D10	8564 VIC-U21
OK	OK	OK	BAD	OK	OK	OK	OK	U39	D9	8564 VIC-U21
OK	OK	OK	BAD	OK	OK	OK	OK	U38	D8	8564 VIC-U21
BAD	OK	OK	BAD	OK	OK	OK	OK	U39	SA0-7	2016 RAM-U19
OK	OK	OK	OK	OK	BAD	OK	OK	U46-53	CAS1	8722 MMU-U7
OK	OK	OK	BAD	OK	OK	OK	OK	U39	GWE	8721 PLA-U11
OK	OK	OK	BAD	OK	OK	OK	OK	U38-40	COLORAM	8721 PLA-U11
OK	OK	OK	BAD	OK	OK	OK	OK	U38,40	GWE	8721 PLA-U11
OK	OK	OK	BAD	OK	OK	OK	OK	U39,41	AEC	8721 PLA-U11

3.2 DIAGNOSTIC COMPLETE TEST WITH NO ERRORS — SCREEN INCORRECT

Although the diagnostic is extremely accurate in detecting hard errors, occasionally the screen may not display correctly and the diagnostic fails to detect the error.

If this seems to be the case, refer to the following listing for the symptom which most resembles the one encountered on the failing system.

IN SOME CASE, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

A LISTED SIGNAL DESIGNATED BY THE '*' IS THE MOST PROBABLE AND SHOULD BE CHECKED FIRST

SYMPTOM		CHECK SIGNAL	OF IC
A.	Diagnostic Characters displayed with no color	CHROMA	8564 VIC-U21
B.	Black Inner Border With Dim Characters	SYNC/LUM	8564 VIC-U21
C.	Characters Scrambled with unreadable screen	VMA0-VMA5/ VA6-VA7	8564 VIC-U21
C.1	Characters may flash, roll or scramble	*VMA0-VMA5	
C.2	Some Tests may be readable		
C.3	Every other character may double e.g., ccllrr rrmm = color ram	*VMA0	
D.	Same characters may display on both left and right side of screen	VMA0-VMA5/ VA6-VA7, *VA6-7	8564 VIC-U21
D.1	Characters scrambled with double cursor displayed during screen ram and/or color ram tests	*VA6-VA7	
E.	Diagnostic Screen fills with random characters except where Diagnostic Information is displayed	SA0-SA7 Random Characters =	CHAR ROM-U18
E.1	Diagnostic Characters may or may not display correctly	0 = SA7 (= SA6 $ = SA5 i = SA3 Solid Blocks = SA4	
F.	Characters flash, sparkle or display incorrectly	SA0-SA7	CHAR ROM-U18
F.1	Characters may be missing the top or bottom dots	*SA0-SA1	
G.	Characters displayed in random colors, no color, characters missing or combination of all	LORAM/HIRAM AEC	8721 PLA-U11
G.1	Count may or may not display correctly e.g. Count = 00 0	*LORAM	
G.2	Color Ram may display 'BAD' with more than one IC flagged (e.g. U39 and U41 Bad)	*AEC	
H.	Diagnostic screen displays random pattern with Top and Bottom halfs different colors, e.g. Top Half Blue, Bottom Half Red	CHAREN	8721 PLA-U11
I.	Diagnostic Screen displays random pattern with screen changing as diagnostic runs	VA14	8721 PLA-U11

3.3 DIAGNOSTIC INTERMITTENT BOOT-UP OR LOCKUP

Normally, a failure on the C128 system is detected by the diagnostic or the prior troubleshooting sections. Occassionally, a system will display random or intermittent problems due to a timing problem or marginal signal.

If this seems to be the case, refer to the following listing for the symptom which most resembles the one encountered on the failing system.

C128 System Diagnostic Symptoms (Continued)

IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

SYMPTOM		CHECK SIGNAL	ON IC
A.	Diagnostic Passes all tests to the Control Port test then locks up	PA0-PA5	6526 CIA-U1
B.	Black screens on both the 40 and 80 colum screens on power up	R/W Z80I/O	8502 MPU-U6 8721 PLA-U11
B.1	Diagnostic intermittently runs with no errors		
C.	Diagnostic locks up during the Noise portion of the sound test	1 MHZ Clock	8564 VIC-U21
D.	Diagnostic intermittently displays one or all of the ram tests bad	PHI IN	8564 VIC-U21
D.1	May complete the entire test or the screen may break up		
E.	Diagnostic locks up during Screen RAM Test	SA0-SA7	CHAR ROM-U18
E.1	Characters may or may not display correctly		
F.	Diagnostic runs to High RAM Bank 0 or High RAM Bank 1 tests then screen fills with white and black squares or random pattern	TA12-TA15	8722 MMU-U7
G.	Diagnostic locks up during Lo RAM Bank 0 or Low RAM Bank 1 test	TA12-TA15	8722 MMU-U7
H.	Diagnostic runs the Port Test Only	40/80	8722 MMU-U7
I.	Top and bottom halfs different colors, e.g., Top Half Blue, Bottom Half Red	CHAREN	8721 PLA-U11
J.	Diagnostic screen displays random pattern with screen changing as diagnostic runs	VA14	8721 PLA-U11
K.	Black screens on both the 40 and 80 column displays	ROM BANK LO ROM BANK HI	8721 PLA-U11
K.1	Intermittently the diagnostic may boot but will run the Port Test only, displaying Kernal, Basic Lo, Basic Hi ROM and PLA — U11 BAD		
L.	Diagnostic normally runs with no errors but may intermittently display one of the Ram Tests and two or more RAM ICs BAD	DWE	8721 PLA-U11
M.	Diagnostic screen sparkles — Red displayed next to all RAM locations inside Red Rectangular Box	CHAROM	8721 PLA-U11
M.1	Red may also be displayed next to PLA Test		
M.2	Sparkles may get worse as Diagnostic runs		
M.3	80 Column power up screen may never clear		

3.4 80 COLUMN DISPLAY PROBLEMS — DIAGNOSTIC NOT INSTALLED

The C128 diagnostic runs in the 40 columns mode only and does not fully test the 80 column display. Normally this does not create any problems as both the 40 and 80 column displays use much the same circuitry, which is tested during diagnostic run time. Normally any 80 column problem will not affect the 40 column mode and almost any problem can be attributed to the 8563 VDC. Unless noted, the 40 column display in the listed symptoms is correct. (Green Outer Border and Black Inner Border)

If this seems to be the case, refer to the following listing for the symptom which most resembles the one encountered on the failing system.

IN SOME CASES, USING THE RESET SWITCH WILL BOOT THE C128 DIAGNOSTIC WHEN NORMAL POWER UP FAILS

A LISTED SIGNAL DESIGNATED BY THE '*' IS THE MOST PROBABLE AND SHOULD BE CHECKED FIRST

	SYMPTOM	CHECK SIGNAL	ON IC
A.	80 Column displays either a solid Black, White or colored snowy screen on power up	DCLK	8563 VDC-U22
B.	80 Column power up message correct with constant vertical roll	VSYN	8563 VDC-U22
C.	80 Column displays power up message with constant horizontal roll	HSYN	8563 VDC-U22
D.	80 Column displays colored crosshatch pattern	R/W	8563 VDC-U22
D.1	Pattern may disappear within 60 seconds		
D.2	80 Column power up pattern may flashes on and off		
E.	80 Column power up message usually correct when the cursor appears, the word 'MONITOR' scrolls down the left side of the screen	LP	8563 VDC-U22
F.	80 Column power up message scrambled	DA0-DA7 *DA0	8563 VDC-U22
G.	80 Column displays full screen of symbols	DA0-DA7	8563 VDC-U22
G.1	Power up message usually displayed but scrambled		
G.2	Block symbols with a dash under each	*DA1	
G.3	Capital 'G' symbols	*DA4	
G.4	Horizontal lines made up of 3 dots, 3 high May have vertical lines in between	*DA5	
G.5	'(' symbols	*DA7	
H.	80 Column displays scrambed power up message	DA0-DA7	8563 VDC-U22
H.1	A second power up message may be displayed half on the right and half on the left side of the screen	*DA2	
I.	80 Column displays cursor only, no power up message	DA0-DA7 *DA3	8563 VDC-U22
J.	80 Column displays 4 random colored vertical patterns on initial power up	DA0-DA7	8563 VDC-U22
J.1	May go to vertical bars next	*DA6	
J.2	Power up message usually scrambled		

C128 System Diagnostic Symptoms (Continued)

SYMPTOM		CHECK SIGNAL	ON IC
K.	80 Column displays full screen of symbols	DD0-DD7	8563 VDC-U22
K.1	Power up message displayed but scrambled		
K.2	May have vertical lines between symbols	*DD0	
K.3	May display only scrambled power up message	*DD0	
K.4	Symbols may be 'i'	*DD0	
K.5	Symbols may be '$'	*DD2	
K.6	Symbols may be '(' usually white	*DD3	
K.7	Symbols may be 'O' Screen may flash on and off	*DD4	
K.8	Symbols may be crosshatch pattern	*DD5	
K.9	Symbols may be [']	*DD5	
L.	80 Column displays scrambled power up message	DD0-DD7	8563 VDC-U22
L.1	Scrambled power up message may be displayed in red	*DD1	
L.2	Scrambled power up message may be displayed in blue	*DD2	
M.	80 Column displays solid colored screen	DD0-DD7	8563 VDC-U22
M.1	Usually solid blue	*DD6	
M.2	Power up message displayed as graphic characters	*DD6	
M.3	Power up message displayed in lower case	*DD7	
N.	80 Column power up pattern flashes on and off	DD0-DD7 *DD6	8563 VDC-U22
	Power up message usually correct	*DD6-DD7	
O.	80 Column power up message displayed in green characters Power up message normal but screen may be dark blue	G	8563 VDC-U22
P.	80 Column power up message displayed in blue	B	8563 VDC-U22
P.1	Power up message normal but screen may be green		
P.2	Power up message normal but screen may be red	R	
Q.	80 Column displays random pattern, (usually	RAS-CAS	8563 VDC-U22
Q.1	Usually crosshatch pattern or vertical lines		
Q.2	May fade out within 60 seconds		
R.	80 Column displays random flashing characters	*CAS	8563 VDC-U22
R.1	Screen may seem split in right and left halfs		
S.	80 Column displays Black screen	CS8563	8563 VDC-U22